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Author Yung-Ming Wang
Author's Email Address No Public.
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Abstract
The genetic algorithm can find an optimal solution in many complex problems, so it has been used widely in many applications, such as image processing, fuzzy control, neural network, communication system, and layout optimization. Genetic algorithm requires very intensive computations in order to perform the optimization. Hence, a dedicated VLSI implementation for it is necessary. We propose a very flexible soft GA IP and its auxiliary software system in this paper. Every module of GA IP is developed by using Verilog hardware description language (HDL), and then is synthesized and verified by the related CAD tools in advance. Those variables in the IP are parameterized as much as possible. With the help of an auxiliary software system named GA Verilog-IP generator, users can choose easily different population sizes, individual lengths, fitness lengths, crossover operations, and mutation rates. Because of the excellent flexibility, the proposed GA IP is very suitable for various real-time GA applications.

The design has been synthesized on Synopsys Design Compiler with the standard-cell from UMC ’s 0.18- cell library. Finally, the layout for the design was generated with the Avant! tools, Apollo (for floorplan, placement and routing), and Dracula (for DRC, ERC and LVS checks). Its core size and gate count are about and 2357.32, respectively. In the simulation, its clock frequency achieves 111 MHz.
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